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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet

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of

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Application Number	09/847,642
Filing Date	May 1, 2001
First Named Inventor	Mihai T. Lazarescu
Group Art Unit	2124
Examiner Name	INGBERG

Attorney Docket Number 261/246

### OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
RGT	AA	Prof. Dov Dori, <u>About OPCAT</u> , 2000, pages 1-2, <a href="http://iew3.technion.ac.il/~dori/opcat/about.htm1">http://iew3.technion.ac.il/~dori/opcat/about.htm1</a>	
RGT	AB	Prof. Dov Dori, <u>OPM Methodology</u> , 2000, pages 1-3, <a href="http://iew3.technion.ac.il/~dori/opcat/methodology.htm1">http://iew3.technion.ac.il/~dori/opcat/methodology.htm1</a>	
RGT	AC	Prof. Dov Dori; <u>OPCAT's Contents</u> , 2000, pages 1-5, <a href="http://iew3.technion.ac.il/~dori/opcat/contents.htm1">http://iew3.technion.ac.il/~dori/opcat/contents.htm1</a>	
RGT	AD	Prof. Dov Dori; <u>Examples</u> , 2000, pages 1-3 <a href="http://iew3.technion.ac.il/~dori/opcat/example.htm1">http://iew3.technion.ac.il/~dori/opcat/example.htm1</a> (Fig. 1 and Fig. 2 did not display when website was viewed).	
RGT	AE	Vojin Zivojinovic, Stefan Pees, Christian Schlaeger, Markus Willems, Rainer Schoenen and Heinrich Moyer, <u>DSP Processor/Compiler Co-Design A quantitative Approach</u> , ICSPAT, 1997, pages 761 - 765	
RGT	AF	Guido Post, Vojin Zivojinovic and Sebastian Ritz, <u>Multiprocessor Architecture Extension for the BlockDiagram-Oriented Design Tool Cossap/Descartes</u> , ICSPAT, 1995	
RGT	AG	Stefan Pees, Vojin Zivojinovic, Andreas Hoffmann, Heinrich Moyer, <u>Retargetable Timed Instruction Set Simulation of Pipelined Processor Architectures</u> , ICSPAT, 1998	
RGT	AH	Marcello Lajolo, Mihai Lazarescu, Alberto Sangiovanni-Vincentelli, <u>A Compilation-based Software Estimation Scheme for Hardware/Software Co-Simulation</u> , CODES, 1999	
RGT	AI	Mihai T. Lazarescu, Jwahar R. Bammal, Edwin Harcourt, Luciano Lavagno, Marcello Lajolo, <u>Compilation-based Software Performance Estimation for System Level Design</u> , HLDVT, November 8, 2000, pages 1-8	
RGT	AJ	Graham R. Hellestrand, <u>Designing System on a Chip Products Using Systems Engineering Tools</u> , 1999, pages 1-6, VaST Systems Technology Corporation	
RGT	AK	Vojin Zivojinovic, Stefan Pees, Heinrich Moyer, <u>LISA - Machine Description Language and Generic Machine Model for HW/SW Co-Design</u> , October 1996, 1996 IEEE Workshop on VLSI Signal Processing, San Francisco	
RGT	AL	Vojin Zivojinovic, Steven Tjian, Heinrich Moyer, <u>Compiled Simulation of Programmable DSP Architectures</u> , 1995, pp. 187-198, In the Proceedings of the 1995 IEEE Workshop on VLSI Singal Processing	
RGT	AM	Vojin Zivojinovic, Juan Martinez Velarde, Christian Schlager, Heinrich Moyer, <u>Integrated Systems for Signal Processing</u> , E.E. Times, October 17, 1994, Issue: 819 pages 1-6, <a href="http://content.techweb.com/se/directlink.cgi?EET18941017S0055">http://content.techweb.com/se/directlink.cgi?EET18941017S0055</a>	
RGT	AN	Vojin Zivojinovic, Stefan Pees, Christian Schlager, Heinrich Moyer, <u>Signal Processing Design</u> , LISA bridges gaps in high-tech languages, E.E. Times, October 7, 1996, Issue: 822, pages 1-6, <a href="http://content.techweb.com/se/directlink.cgi?EET199601007S0138">http://content.techweb.com/se/directlink.cgi?EET199601007S0138</a>	
RGT	AO	V. Zivojinovic, S. Pees, <u>Compiled DSPs check out fast</u> , E.E. Times, October 23, 1995, Issue: 871, Section: Digital Signal Processing, Pages 1-5, <a href="http://content.techweb.com/se/directlink.cgi?EET19951023S0056">http://content.techweb.com/se/directlink.cgi?EET19951023S0056</a>	
RGT	AP	Vojin Zivojinovic, Heinrich Moyer, <u>Compiled HW/SW Co-Simulation</u> , 1996, Integrated Systems for Signal Processing, Aachen University of Technology, Aachen, Germany	
RGT	AQ	Dr. Graham Hellestrand, <u>The Advent of the Virtual Processor Model</u> , E. E. Times, May 14, 1999, pages 1-7, VaST Systems Technology, Santa Clara, CA, USA	
RGT	AR	Graham R. Hellestrand, <u>Systems Engineering: The Era of the Virtual Processor Model (VPM)</u> , April 14, 1999, pages 1-6, VaST Systems Technology, Santa Clara, CA, USA	
RGT	AS	Stephan Ohr, <u>Nonlinear Tips Analog Synthesis</u> , E. E. Times, June 12, 2001, Pages 1-3, Com, <a href="http://www.eetimes.com/story/OEG20010612S0067">http://www.eetimes.com/story/OEG20010612S0067</a>	

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Group Art Unit	2124
Examiner Name	I W GIBERG

Sheet	2	of	2	Attorney Docket Number	261/246
<i>PL TR</i>	AT	Soner Önder, Rajiv Gupta, <u>Automatic Generation of Microarchitecture Simulators</u> , May 1998, IEEE International Conference on Computer Languages			
<i>PL FF</i>	AU	Joachim Fitzner, Chris Schlager, Davorin Mista, Vojin Zivojinovic, <u>Implementing LISA Tools Based on a DSP Architecture Description</u> , ICSPAT 1999			
<i>PL AV</i>	AV	Lisa Guerra, Joachim Fitzner, Dipankar Talukdar, Chris Schlager, Bassam Tabbara, Vojin Zivojinovic, <u>Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification</u> DAC 1999			
<i>PL AW</i>	AW	Stefan Pees, Andreas Hoffmann, Vojin Zivojinovic, Heinrich Meyr, <u>LISA - Machine Description Language for Cycle-Accurate Models of Programmable DSP Architectures</u> , DAC 1999			
<i>PL AX</i>	AX	Chris Schlager, Joachim Fitzner, Vojin Zivojinovic, <u>Using Supersim Compiled Processor Models for Hardware, Software and System Design</u> , ICSPAT 1998			
<i>PL AY</i>	AY	Vojin Zivojinovic, Chris Schlager, Joachim Fitzner, <u>System-Level Modeling of DSP and Embedded Processors</u> , ASIOMAR 1998			

Examiner  
Signature*Christopher Russ*Date  
Considered*5/10/05*

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